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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Docket: HP10981866-1	App: 09/378,596
		Applicant: Gupta et al.	
		Filed: August 20, 1999	RECEIVED Art No: Nov 20 1999 Group 2700
OTHER DOCUMENTS			
<i>O P E JC33</i>	<i>NOV 16 1999</i>	Reiner Leupers, Peter Marwedel, "Retargetable Generation of Code Selectors from HDL Processor Models," IEEE, 1997, pp.140-144.	
<i>Patent & Trademark Office</i>		George Hadjiiannis, Silvina Hanono, Srinivas Devadas, "ISDL: An Instruction Set Description Language for Retargetability," ACM, 1997, pp. 299-302.	
<i>Olen</i>		Gyllenhaal et al., "HMDES Version 2.0 Specification," Hewlett Packard Laboratories Technical Report IMPACT-96-3,	
<i>Olen</i>		Hadjiiannis et al., "A Methodology for Accurate Performance Evaluation in Architecture Exploration."	
<i>Olen</i>		Hoogerbrugge et al., "Automatic Synthesis of Transport Triggered Processors."	
<i>Olen</i>		Corporaal et al., "MOVE: A Framework for High-Performance Processor Design," ACM, 1991, pp. 692-701	
<i>Olen</i>		Corporaal et al., "Cosynthesis with the MOVE Framework."	
<i>Olen</i>		Lanneer et al, "Chapter 5 - Chess: Retargetable Code Generation for Embedded DSP Processors," Code Generation for Embedded Processors, Kluwer Academic Publications, pp. 85-102.	
<i>Olen</i>		Fauth, "Chapter 8 - Beyond Tool-Specific Machine Descriptions," Code Generation for Embedded Processors, Kluwer Academic Publications, pp. 138-152.	
<i>Olen</i>		G. J. Chaitin, "Register Allocation & Spilling Via Graph Coloring," ACM, 1982, pp. 98-105.	
<i>Olen</i>		Fisher et al., "Custom-Fit Processors: Letting Applications Define Architectures," 29 th Annual Conference IEEE/ACM International Symposium on Microarchitecture, December 2-4, 1996, Paris, France, pp. 324-336.	
EXAMINER:	<i>Olen</i>	DATE 9/15/02	
* Examiner: Initial if considered, whether or not in conformance with MPEP 60; draw line through cite if not in conformance and not considered. Send copy.			

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PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		ATTY. DOCKET NO. hp10981866-1	SERIAL NO. 09/378,596
		APPLICANT Gupta et al.	
		FILING DATE 8/20/99	GROUP RECEIVED NOV 20 1999

REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS			
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS Group 2 SUB CLASS
	1A				
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

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PATENT & TRADEMARK OFFICE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION
							YES NO
	1L						
	1M						
	1N						
	1O						
	1P						

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

<i>See</i>	1Q	Aditya et al., "Elcor's Machine Description System: Version 3.0," HPL-98-128, October 1998, pp. 1-75.
	1R	Rau et al., "Machine-Description Driven Compilers for EPIC Processors," HP Laboratories Technical Report, HPL-98-40, September 1998, pp. 1-82.
<i>See</i>	1S	Kathail et al., "HPL PlayDoh Architecture Specification: Version 1.0," HP Laboratories Technical Report, HPL-93-80, February 1994, pp. 1-48.

EXAMINER <i>See</i>	DATE CONSIDERED 9/15/02
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PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1469

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.	APPLICATION NO.	CONFIRMATION NO.
10981866-1	09/378,596	
APPLICANT		
Gupta, Shail Aditya, et al		
FILING DATE	GROUP	
8/20/1999		

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
SL	1A US6,226,776	5/1/2001	Yuri V. Panchul, et al	716	3
	1B				
	1C				
	1D				
	1E				
	1F				
	1G				
	1H				
	1I				
	1J				
	1K				

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION
							YES
		1L					
		1M					
		1N					
		1O					
		1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	
	1R	
	1S	

EXAMINER

DATE CONSIDERED

9/15/02